Electronic Version
Stylesheet Version v1.1.1

VERY LONG INSTRUCTION WORD ARCHITECTURE

Abstract

A very long instruction word (VLIW) architecture has a VLIW input port for sequentially inputting a plurality of VLIWs, a decoder for decoding a plurality of instructions of the VLIWs, at least a register, a plurality of data buses, a plurality of arithmetic logic units (ALUs) for executing the instructions, and a plurality of multiplexers. Each output port of the multiplexers is connected to one of the ALUs, and each input port of the multiplexers is connected to the register and output ports of the ALUs via the data buses. Each of the multiplexers selects two outputs from the outputs of the register and the ALUs so that the connected ALU executes one of the instructions to operate the two selected outputs.